19. A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

securing said first stacking surface to said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad;

electrically coupling said first semiconductor die to said second semiconductor die with at least one topographic contact extending from a conductive bond pad on said second active surface to a conductive bond pad on said first active surface.

20. A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes at least one conductive bond pad;

electrically coupling said first active surface to said substrate with at least one topographic contact extending from a conductive bond pad on said first active surface to a conductive contact on said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes at least one conductive bond pad; and

securing said first stacking surface to said second stacking surface.

21. A method of stacking a plurality of semiconductor die, said method comprising:

providing a substrate;

providing a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

providing a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

interposing said first semiconductor die between said substrate and said second semiconductor die such that a surface of said second semiconductor die defines an uppermost die surface of said multiple die semiconductor assembly and such that a surface of said first semiconductor die defines a lowermost die surface of said multiple die semiconductor assembly;

securing at least one decoupling capacitor to said uppermost die surface; and

conductively coupling said decoupling capacitor to at least one of said first and second semiconductor dies.

22. A method of stacking a plurality of semiconductor die along a cross section, said method comprising:

providing a substrate;

positioning a first semiconductor die adjacent said substrate relative to said cross section;

positioning a second semiconductor die adjacent said first semiconductor die relative to said cross section;

interposing said first semiconductor die between said substrate and said second semiconductor die relative to said cross section;

positioning at least one decoupling capacitor adjacent said second semiconductor die relative to said cross section;

securing said decoupling capacitor to said second semiconductor die; and

interposing said second semiconductor die is between said decoupling capacitor and said first semiconductor die relative to said cross section.

23. A method of assembling a printed circuit board, said method comprising:

providing a substrate including first and second surfaces and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface,

said first active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads;

securing said first stacking surface to said first surface of said substrate between said conductive contacts included on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface, and

said second active surface includes a plurality of conductive bond pads;

electrically coupling said first semiconductor die to said second semiconductor die with a plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

securing a single decoupling capacitor to said second stacking surface;

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said first active surface, and a conductive contact on said first surface of said substrate;

electrically coupling said bond pad on said first active surface to said second semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said second active surface to a corresponding conductive bond pad on said first active surface;

arranging said pair of conductive lines such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said second surface of said substrate to said first surface of said printed circuit board.

24. A method of assembling a printed circuit board, said method comprising:

providing a substrate including a first surface and conductive contacts included on said first surface;

providing a first semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said first die defines a first active surface,

the other of said major surfaces of said first die defines a first stacking surface, and

said first active surface includes a plurality of conductive bond pads;

electrically coupling said first active surface to said substrate with a plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

providing a second semiconductor die including a pair of major surfaces, wherein

one of said pair of major surfaces of said second die defines a second active surface,

the other of said major surfaces of said second die defines a second stacking surface,

said second active surface includes a plurality of conductive bond pads, and

said first stacking surface is devoid of conductive bond pads;

securing said first stacking surface to said second stacking surface;

securing a single decoupling capacitor to said second stacking surface;

providing a pair of conductive lines, each of said conductive lines connecting a terminal of said decoupling capacitor, a bond pad on said second active surface, and a conductive contact on said first surface of said substrate;

electrically coupling said conductive contact on said first surface of said substrate to said first semiconductor die via one of said plurality of topographic contacts extending from respective conductive bond pads on said first active surface to corresponding conductive contacts on said first surface of said substrate;

arranging said pair of conductive lines such that said decoupling capacitor is connected across V_{ss} and V_{cc} pins of said first and second semiconductor dies;

positioning a printed circuit board such that a first surface of said printed circuit board faces said substrate; and

providing a plurality of topographic contacts extending from said substrate to said first surface of said printed circuit board.

25-44. (Canceled)

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45. A method of stacking a plurality of semiconductor die as claimed in claim 19 wherein said first semiconductor die is secured to said substrate by interposing a layer of die attach adhesive between said substrate and said first semiconductor die.

46. A method of stacking a plurality of semiconductor die as claimed in claim 19 wherein an encapsulant is formed over at least a portion of said first semiconductor die, at least a portion of said second semiconductor die, and at least a portion of said substrate.

47. A method of stacking a plurality of semiconductor die as claimed in claim 19 wherein said first semiconductor die is electrically coupled to said substrate.

48. A method of stacking a plurality of semiconductor die as claimed in claim 19 wherein said second semiconductor die is electrically coupled to said substrate.

49. A method of stacking a plurality of semiconductor die as claimed in claim 19 wherein said first semiconductor die and said second semiconductor die are electrically coupled to said substrate.

50. A method of stacking a plurality of semiconductor die as claimed in claim 20 wherein said first die is spaced from substrate by said topographic contact.

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51. A method of stacking a plurality of semiconductor die as claimed in claim 22 wherein said first semiconductor die is positioned directly adjacent said substrate within said cross section.

REMARKS

By the present amendment, claims 1-18 and 25-44 have been canceled. Original claims 19-24 and new dependent claims 45-51 are pending in the present application. Claims 1-44 were the subject of a Restriction Requirement in the in parent application serial no. 09/804,421. Claims 1-18 and 25-44 were elected for substantive examination in the parent application, while claims 19-24 were withdrawn from consideration.

CONCLUSION

Applicants respectfully submit that the application is in condition for allowance. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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